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APPENDIX - A

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the claims:

Please cancel claims 2-3.

Please amend the following claims:

1. A packaged semiconductor device comprising:
a semiconductor chip;
a laminate defining first and second major faces, said laminate including
an electrically conductive layer,
an underlying substrate supporting said electrically conductive layer, and
at least one void formed in said laminate so as to extend from [one of said major faces] said first major face through said electrically conductive layer [at least as far as said underlying substrate], through said underlying substrate and through said second major face; and
an encapsulant positioned to mechanically couple said semiconductor die to said laminate, wherein said encapsulant is further positioned to extend through said void from said first major face to said second major face and contacting [into said void so as to contact] said underlying substrate.

4. A packaged semiconductor device as claimed in claim 1 wherein said contact between said encapsulant and said underlying substrate is characterized by an adhesive bond.

5. A packaged semiconductor device as claimed in claim 1 wherein said encapsulant occupies substantially all of said void.

6. A packaged semiconductor device as claimed in claim 1 wherein said semiconductor chip is supported by said laminate and wherein said encapsulant and said laminate are arranged to enclose substantially all of said semiconductor chip.

7. A packaged semiconductor device comprising:
a semiconductor chip;
a laminate defining first and second major faces, said laminate including
a solder resist layer,
an underlying substrate,
an electrically conductive layer interposed between said solder resist layer and said underlying substrate, and
at least one void formed in said laminate so as to extend from said first major face [one of said major faces] through said solder resist layer, [and] through said electrically conductive layer, through [at least as far as] said underlying substrate and through said second major face; and
an encapsulant positioned to mechanically couple said semiconductor die to said laminate, wherein said encapsulant is further positioned to extend into said void so as to contact said underlying substrate.

8. A packaged semiconductor device comprising:
a semiconductor chip;
a laminate defining first and second major faces and including a plurality of laminated layers, said laminate including at least one void formed therein so as to extend from one of said major faces through a plurality of said laminated layers; and
an encapsulant positioned to mechanically couple said semiconductor die to said laminate, wherein said encapsulant is further positioned to extend into said void across said plurality of laminated layers so as to contact a portion of said laminate between said first and second major faces of said laminate.

9. A packaged semiconductor device as claimed in claim 8 wherein said at least one void extends from said first major face through said laminate to said second major face and wherein said encapsulant is positioned to extend through said void from said first major face to said second major face.

10. A packaged semiconductor device as claimed in claim 8 wherein said contact between said encapsulant and said laminate is characterized by an adhesive bond.

11. A packaged semiconductor device as claimed in claim 8 wherein said encapsulant occupies substantially all of said void.

12. A packaged semiconductor device as claimed in claim 8 wherein said semiconductor chip is supported by said laminate and wherein said encapsulant and said laminate are arranged to enclose substantially all of said semiconductor chip.

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13. A packaged semiconductor device comprising:
a semiconductor chip;
an FR-4 epoxy-glass laminate [a prepreg epoxy resin glass cloth laminate] defining first and second major faces and including a plurality of laminated epoxy [prepreg] layers, said epoxy [prepreg] laminate including at least one void formed therein so as to extend from one of said major faces through a plurality of said laminated epoxy [prepreg] layers; and
an encapsulant positioned to mechanically couple said semiconductor die to said epoxy [prepreg] resin glass-cloth laminate, wherein said encapsulant is further positioned to extend into said void across said plurality of laminated epoxy [prepreg] layers so as to contact a portion of said laminate between said first and second major faces of said laminate.

23. A computer including at least one packaged semiconductor device comprising:
a semiconductor chip;
a laminate defining first and second major faces, said laminate including
an electrically conductive layer,
an underlying substrate supporting said electrically conductive layer,
at least one void formed in said laminate so as to extend from said first major face [one of said major faces] through said electrically conductive layer, through [at least as far as] said underlying substrate, and through said second major face; and
an encapsulant positioned to mechanically couple said semiconductor die to said laminate, wherein said encapsulant is further positioned to extend into said void so as to contact said underlying substrate.